REMARKS

Summary of the Office Action

Claims 1, 2, 4-8, and 10-12 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Shirai (US 6,482,697 B1).

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Shirai.

The drawings are objected to under 37 C.F.R. § 1.83(a).

Claim 7 is objected to for minor informalities.

Summary of the Response to the Office Action

Applicants have amended claims 1 and 7. Accordingly, claims 1-12 are pending for consideration.

Objection to the Drawings

The drawings are objected to under 37 C.F.R. § 1.83(a) for not showing every features of the invention specified in the claims. Specifically, the Office Action alleges that the features of claim 7, lines 11-15 are not shown. Applicants have amended claim 7 to recite a "method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region." Accordingly, Applicants respectfully submit that the code address memory cell in a peripheral circuit region is shown in FIG. 4, and the flash memory cell in a cell region is shown in FIG. 2. Thus, Applicants respectfully assert that every feature of claim 7 is shown in FIGs. 2 and 4, and respectfully request that the objection to the drawings under 37 C.F.R. § 1.83(a) be withdrawn.

Objection to the Claims

Claim 7 is objected to for minor informalities. Accordingly, Applicants have amended claim 7 in accordance with the Examiner's suggestions. Thus, Applicants respectfully request that the objection to claim 7 be withdrawn.

All Claims Define Allowable Subject Matter

Claims 1, 2, 4-8, and 10-12 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Shirai (US 6,482,697 B1), and claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Shirai. Applicants respectfully traverse these rejections as being based upon a prior art reference that neither teaches nor suggests the novel combination of features recited in amended independent claims 1 and 7, and hence dependent claims 2-6 and 8-12.

Independent claim 1, as amended, recites at least the step of "forming a gate insulating film in which a plurality of oxide films and nitride films are stacked on a surface of a semiconductor substrate." Applicants respectfully submit that the ONO inter-gate insulator 108 of Shirai cannot correspond to the "gate insulating film," as recited by claim 1. In contrast to Applicants' claimed invention, Shirai teaches, in FIGs. 5A to 5L, sequential steps of forming the ONO inter-gate insulator 108 on both the polycrystalline silicon capacitive electrode layer 107 and the first inter-layer insulator 110. Accordingly, Applicants respectfully assert that Shirai does not teach or suggest at least the step of "forming a gate insulating film in which a plurality of oxide films and nitride films are stacked on a surface of a semiconductor substrate," as recited by amended independent claim 1.

Independent claim 7, as amended, recites at least the step of "patterning said second polysilicon film and said insulating film so that they can remain only in a given region of said cell region and said peripheral circuit region, thus forming a control gate on the floating gate in said cell region, and a gate on a surface of the substrate in said peripheral circuit region." Applicants respectfully submit that the ONO inter-gate insulator 108 of Shirai cannot correspond to the "gate insulating film," as recited by amended independent claim 7.

In contrast to Applicants' claimed invention, Shirai teaches, in FIG. 6 and at col. 20, lines 40-43, that the MOSFETs in the peripheral circuit area are formed using the same processes used to form the memory cells in the memory cell area. Accordingly, as shown in FIG. 6 of Shirai, the gate structures 125 within the peripheral circuit are the same as the gate structures 125 within the memory circuit area. Thus, Applicants respectfully assert that the ONO inter-gate insulator 108 in FIGs. 5A-5L of Shirai is not provided on a surface of the substrate 101 in the peripheral circuit area. Therefore, Applicants respectfully assert that Shirai does not teach or suggest at least the step of "patterning said second polysilicon film and said insulating film so that they can remain only in a given region of said cell region and said peripheral circuit region, thus forming a control gate on the floating gate in said cell region, and a gate on a surface of the substrate in said peripheral circuit region," as recited by amended independent claim 7.

Applicants further assert that claims 2-6 and 8-12 are patentable at least because of their dependence upon independent claims 1 and 7, respectively, as well as the individual features each of claims 2-6 and 8-12 recite.

For at least the above reasons, Applicants respectfully submit that the features of claims 1-12 are neither taught nor suggested by Shirai. Thus, Applicants respectfully assert that the rejections under 35 U.S.C. §§ 102(e) and 103(a) should be withdrawn because the above-discussed novel combination of features recited by claims 1-12.

CONCLUSION

In view of the foregoing, Applicants respectfully request reconsideration and the timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicants' undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

By: Mary Jane Boswell
Mary Jane Boswell
Reg. No. 33,652

Dated:

CUSTOMER NO. 009629
MORGAN, LEWIS & BOCKIUS LLP
1111 Pennsylvania Avenue, N.W.
Washington, DC 20004